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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SNELL & WILMER
ONE ARIZONA CENTER
400 EAST VAN BUREN
PHOENIX, AZ 850040001

EXAMINER
LEADER, WILLIAM T

ART UNIT	PAPER NUMBER
1742	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,598	EMESH ET AL.	
	Examiner	Art Unit	
	William T. Leader	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/17/04; 5/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Ashjaee et al (6,482,307).

3. The Ashjaee et al patent discloses apparatus for electroplating or electropolishing semiconductors wafers. As shown in figure 4 (described at column 3, line 34 to column 4, line 33), the apparatus includes pad 8 and anode 9 which has an electrically conductive surface proximate to the pad. Anode 9 includes holes 24 which accommodate pins 20 which are electrically isolated from the anode plate by an insulator 26. The pins are part of a cathode plate 30, and correspond to the electrically conducting element recited in instant claim 1. By extending through the holes in the anode, pins 20 are disposed within the electrically conductive surface as recited in claim 1. The apparatus positions wafer 16 against pad 8. A power source is provided which supplies electrical power. Figure 4 illustrates a positive voltage (+) being applied to the anode, and a negative voltage (-) being applied to the

cathode plate and pins 20. This polarity provides electroplating and is opposite to that recited in claim 1. However, Ashjaee et al disclose that copper may be either plated onto or removed from the wafer, depending on the polarity of the wafer, and that circuitry used for inverting the polarity of the potential is well known and commonly used (column 4, lines 29-33). With reversed polarity, anode 9 would function as a cathode. Thus all elements of the apparatus recited in claim 1 are taught by Ashjaee et al.

4. Claim 3 recites that at least one conducting element is positioned above a top surface of the polishing pad. Figure 4 shows pins 20 at a height above pad 8. Claim 2 recites at least one conducting element is positioned flush with a top surface of the polishing pad. Ashjaee et al disclose that cathode plate 20 is spring loaded by springs 32 which bias the tips of pins 20 toward the wafer surface during operation. The gap 34 between pad 8 and the surface of the wafer may be adjusted or the pad may contact the wafer surface. The pressure with which the wafer and pad touch each other may be adjusted (column 4, lines 9-13). When both the tips of the pins and the pad contact the surface of the wafer, the pins will be flush with the top of the pad as recited in claim 2. Claim 4 recites at least one conducting element is positioned below a top surface of the polishing pad. Ashjaee et al disclose that the electrical contacts can touch the front side of the wafer in order to make contact or can make contact without touching the wafer by way of a "field effect" (column 7,

lines 53-56). In this instance, the pad would touch the wafer but the tips of pins 20 would not -- they would be below the surface as recited in claim 4.

5. Claim 5 recites that the conducting elements are positioned such that a uniform electric potential gradient is created across the wafer. Ashjaee et al disclose that a plurality of contacts distributed all over the wafer surface may be used. As the number of contacts increases, the voltage drop from the center to the edge of the wafer will become smaller and the thickness of the plated metal becomes more uniform (column 5, lines 17-33). Thus, Ashjaee et al teach a structure of the apparatus which would provide a uniform electric potential gradient across the wafer in use.

6. Ashjaee et al disclose that the pins can be made of refractory metals such as Mo, Ta and W. These metals would exhibit low electrical contact resistance and resistance to corrosion as recited in claim 6.

7. Claim 10 recites that the metallized surface of the workpiece does not contact the electrically conductive surface during removal. The limitation of claim 10 is written as a process limitation which describes a relationship between the apparatus and the workpiece during use of the apparatus. Claim 10 is interpreted as reciting apparatus which is capable of operating in the manner recited. By disclosing the presence of pad 8 between the workpiece and the electrically conductive surface of anode (cathode) 9, the Ashjaee et al patent meets this limitation.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashjaee et al in view of Marmillion et al (5,943,977) and Zubak (3,849,272).

11. Ashjaee et al is silent as to the spacing between anode (cathode) 9 and the metallized surface of the wafer. Claims 7-9 differ from Ashjaee et al by reciting ranges for the spacing. The Marmillion et al patent is directed to a method of

planarizing a workpiece such as a wafer. As in the apparatus of Ashjaee et al, the wafer in the apparatus of Marmillion may be pressed against a pad supported by the surface of the adjacent element, in this case the platen. Since both the conductive surface and the metallized surface of the wafer contact the pad, the spacing can be no greater than the thickness of the pad. Marmillion et al teach that the pad may be made of a porous resilient material such as polyurethane and may have a thickness of 0.06mm (column 4, lines 48-54). Since the pad is made of a resilient material, the pressure applied during the process would be expected to further reduce the thickness of the pad and the distance between the platen and the surface of the workpiece. The spacing used by Marmillion et al falls within the ranges recited in claims 7 and 8. The Zubak patent is directed to a process for the electrochemical removal of material from a workpiece. Zubak teaches that to improve accuracy it is known to reduce the thickness of the working gap to the utmost (column 1, lines 28-30). It would have been obvious at the time the invention was made to have minimized the working gap between the anode (cathode) 9 and the surface of the workpiece in Ashjaee et al to a small value as taught by Marmillion et al and Zubak to improve the accuracy of the material removal.

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent

the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 1-10 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-36 and 59-69 of U.S. Patent No. 6,736,952. Although the conflicting claims are not identical, they are not patentably distinct from each other because instant claim 1 recites limitations which are the same as those recited in claim 59 of the patent but with some limitations removed. Thus, claim 1 is broader than claim 59 of the patent and includes the subject matter of claim 59 within its scope.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 571-272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 571-272-1244. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WL
William Leader
September 20, 2004

ROY KING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700